## REMARKS

Claims 1-8 were examined and reported in the Office Action. Claims 1-8 are rejected. Claims 1 and 6 are amended. Claims 2-5 and 8 are cancelled. Claims 1 and 6-7 remain.

Applicants request reconsideration of the application in view of the following remarks.

### I. In the Drawings

It is asserted in the Office Action that the drawings are objected to. Applicant has cancelled claim 8 to overcome the objection. Approval is respectfully requested.

### II. 35 U.S.C. §102(e)

It is asserted in the Office Action that claims 1,2 and 7 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,909,523 issued to Sakaino ("Sakaino"). Applicant respectfully disagrees.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] submount for an opto-electronic module for outputting light incident from an opto-electronic device as an electrical signal, the submount comprising: a dielectric material having a polygonal shape with a front face and a bottom face; and an interconnection line having a coplanar

waveguide structure, attached to the front face and the bottom face of the dielectric material, and electrically connected to the opto-electronic device to output signals from the opto-electronic device, the coplanar waveguide structure includes a plurality of interconnection lines, which are spaced apart from each other, the interconnection lines are a first ground line, a signal transmission line, a second ground line, and a bias application line, respectively, which are sequentially disposed, wherein the opto-electronic device is attached to a portion of the second ground line, which is attached to the front face of the dielectric material, and the opto-electronic device is also connected to the signal transmission line and the bias application line via wires."

Applicant's claim 7 contains the limitations of "[a] packaging method using a submount for an opto-electronic module including a dielectric material and an interconnection line having a coplanar waveguide structure, the packaging method comprising: (a) attaching an opto-electronic device to the interconnection line to electrically connect the opto-electronic device to the interconnection line; and (b) attaching the interconnection line, to which the opto-electronic device is attached, to a conductive interconnection line of a substrate."

In Applicant's claimed invention, an opto-electronic device 230 is attached to a second ground 223 and electrically coupled to a signal transmission line 222 and a bias application line 224 via wires 240. Therefore, the surface of the second ground line 223, which is an electrical reference plane of an electrical signal applied to wires 240, is disposed on the base planes of wires 240. Thus, the effects caused by parasitic components, such as inductance attributed to wires 240, are minimized.

Saikano discloses optical module in which an optical fiber or an optical waveguide is optically connected with an optical semiconductor device. The optical module is used in an optical transmitter or receiver. Saikano, however, does not teach, disclose or suggest the limitations of Applicant's amended claim 1 of "a dielectric material having a polygonal shape with a front face and a bottom face; and an interconnection line having a coplanar waveguide structure, attached to the front face and the bottom face of the dielectric material, and electrically connected to the

opto-electronic device to output signals from the opto-electronic device, the coplanar waveguide structure includes a plurality of interconnection lines, which are spaced apart from each other, the interconnection lines are a first ground line, a signal transmission line, a second ground line, and a bias application line, respectively, which are sequentially disposed, wherein the opto-electronic device is attached to a portion of the second ground line, which is attached to the front face of the dielectric material, and the opto-electronic device is also connected to the signal transmission line and the bias application line via wires." Further, the device disclosed by Saikano does not teach, based on the structure of Applicant's claimed invention, that the effects caused by parasitic components, such as inductance attributed to wires (e.g., wires 240), are minimized.

Regarding Applicant's claim 7, Saikano discloses that block 21 is disposed on the upper surface 81b of substrate 81, and connected to the substrate by the wires (not shown). (See Saikano, Figures 1 and 4). Distinguishable, in Applicant's claimed invention interconnection line 220 in opto-electronic module 200 is connected directly to conductive interconnection line 420 of substrate 410. Therefore, Saikano does not teach, disclose or suggest the limitations contained in Applicant's claim 7 of "attaching an opto-electronic device to the interconnection line to electrically connect the opto-electronic device to the interconnection line; and (b) attaching the interconnection line, to which the opto-electronic device is attached, to a conductive interconnection line of a substrate."

Thus, Saikano does not disclose, teach or suggest the limitations contained in Applicant's amended claims 1 and 7, as listed above. Since Saikano does not disclose, teach or suggest all of Applicant's amended claims 1 and 7 respective limitations, as listed above, Applicant respectfully asserts that a prima facie rejection under 35 U.S.C. §102(b) has not been adequately set forth relative to Saikano. Thus, Applicant's amended claims 1 and 7 are not anticipated by Saikano. Additionally, the claim that directly depends on Applicant's claim 1, namely claim 6, is also not anticipated by Saikano for the above same reasons.

Accordingly, withdrawal of the 35 U.S.C. §102(b) rejection for claims 1,2 and 7 are respectfully requested.

## III. 35 U.S.C. §103(a)

It is asserted in the Office Action that claims 3-5 and 8 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 5,909,523 issued to Sakaino et al. ("Sakaino"). Applicant has cancelled claims 3-5 and 8.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 3-5 and 8 are respectfully requested.

## CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1 and 6-7, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office, Commissioner for Patents, Mail Stop Non-Fee Amendment, Post Office Box 1450, Alexandria, Virginia 22313-1450, on the date shown below.

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Jean Svoboda March 12, 2004